

What semiconductors are available in the 10 kW NPC2 inverter reference design?

Figures 3,4,5,6 and 7 show the stand-alone REF-10KW3LNPC2, ISODRV-3240C4P15N05-1, PB-APS-24V-5V ISO, REF-10KW3LNPC2-Filter and PB-CAPTANK-1.1KV. Figure 8 shows the main semiconductors offered in the 10 kW NPC2 inverter reference design. This chapter lists the features available for the 10 kW NPC2 inverter reference design.

Which boards work together to form a three-phase inverter reference design?

The following boards work in tandem to form this three-phase inverter reference design: The UCC21710 device is a 5.7-kVRMS, reinforced isolated gate driver for Insulated-Gate Bipolar Transistors (IGBT) and SiC MOSFETs with split outputs, providing 10-A source and 10-A sink current.

How much power does a 10 kW inverter have?

The final design dimensions are outlined in Table 3-11 and show a total volume of 7 L. With a power rating of 10 kW, this results in a power density of 1.44 kW/L. The following sections cover the results for the inverter mode and PFC mode of operation. Section 3.2.5.1.1 shows the results when the converter is operated in the PFC mode.

How does a 10 kW NPC2 inverter work?

The 10 kW NPC2 inverter reference design follows a hot-side control structure where all the measurements and the gate-drive power supply offer functional isolation. Two microcontrollers are used then on the board where one is responsible for the control of the converter.

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ABSTRACT This application note presents a detailed solution for implementing a 3-phase solar inverter application system based on the TMS320F28035 microcontrollers ...

10kW 3-phase 3-level T-type inverter reference design for solar string inverter TIDA-01606 ??? ???? ????
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The C2000Ware Digital Power SDK (DPSDK) is a cohesive set of reference design solutions, tools, and documentation designed to minimize development time of C2000 MCU ...

This reference design provides an overview on how to implement a bidirectional three-level, three-phase, SiC-based active front end (AFE) inverter and power factor correction (PFC) stage.

This reference design provides an overview into the implementation of a GaN-based single-phase string

